## Remarks

In an Office Action dated January 30, 2006, the examiner rejected claims 1-3, 8-11, 13-15, 23, 25, 26, 28 and 29 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,938,530 to Watanabe. Claims 4-7, 12, 16-22, 24, and 27 are apparently allowable over Watanabe.

The examiner also rejected claims 1-26 under 35 U.S.C. § 102(e) as being anticipated by published U.S. Patent Application No. 2005/0041031 to Diard.

In response, applicants have amended claims 1, 2, 4, 5, 7, 10-12, 15, and 19-23, and added new claims 30-39. Claims 1-39 are pending for consideration.

A. <u>Antedating U.S. Patent Application No. 2005/0041031 to Diard</u>

U.S. Patent Application No. 2005/0041031 to Diard has a filing date of August 18, 2003. Attached herewith is an Inventors' Declaration submitted under 37 C.F.R.§ 1.131 declaring that the date of invention for the subject matter of the present application is before this date. Thus, U.S. Patent Application No. 2005/0041031 is removed as a reference.

In submitted this declaration, applicants do not expressly or implicitly acknowledge the veracity or correctness of the examiner's position that a graphics processor somehow anticipates the claimed invention. Quite to the contrary, applicants utterly reject this suggestion. Nonetheless, to expedite allowance of the pending claims, applicants hereby remove the Diard application as a reference in relation to the subject application.

B. <u>Traversing the anticipation rejection over U.S. Patent No. 5.938,530</u>

The examiner's rejection of claims 1-3, 8-11, 13-15, 23, 25, 26, 28 and 29 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,938,530 to Watanabe is entirely predicated upon multiple erroneous assumptions and interpretations.

The most grievous of these misinterpretations relates to the term "Physics Processing Unit (PPU)." The Office Action identifies, without accompanying explanation or support, "co-processor 108" in the Watanabe document as a putative PPU. This gross misinterpretation of an important claim element coupled with the examiner's

amazing (and equally erroneous) laundry list of "inherency" conclusions serve to effectively assume away applicants entire invention. In so doing, the examiner utterly ignores everything taught in the subject application.

A more careful reading of the Watanabe document reveals that co-processor 108 is nothing more than a conventional, floating-point co-processor connected to CPU 101. (See, Watanabe at Col. 3, line 65 through Col. 4, line 2). Math co-processors have been commercially available in desktop computers, for example, since the early 1980's. Floating point computations have been commonly performed by co-processors like the Intel 8087 for several decades now, as one way of alleviating the computational burden placed an associated CPU.

However, applicants do not claim a conventional combination of a CPU with a generic, floating point co-processor as the Office Action suggests. The subject application makes this point very clear:

> The digital calculation of physics simulation data involves a considerable quantity of mathematical procedures referred to as "floating point" operations. Ideally, the great multiplicity of floating point operations required to calculate physics simulation data would done efficiently and at a greatly reduced price point over the conventional, software-based practice. That is, a maximum number of floating point operation per unit cost is highly desired.
>
> **However, the efficient calculation of floating point data in and of itself is not enough**. Once calculated, the physics simulation data must be efficiently communicated from the calculation means to the host device (e.g., a PC or game console with its associated applications). Thus, a well conceived architecture is required that incorporates the specialized hardware resources and data transfer mechanisms required to efficiently calculate physics simulation data and communicate it to the host. In other words, the architecture must provide not only increased floating point operations, but also the right mix of floating point operations capability and data throughput. It must also avoid data stalls, and long latency periods during which data is loaded and unloaded from the circuitry executing the floating point operations.

(See, the subject specification at page 8, emphasis added).

Certainly, the PPU of the claimed invention may take many different forms, but any PPU must at a minimum be adapted to generate and provide "physics simulation data" sufficient to implement complex, real-time, physics effects. (See, for example, the subject specification at page 13). This can not be said of a conventional math co-processor. However implemented, "the PPU . . . [is] designed to efficiently provide physics simulation data and communicate this data to the CPU." (See, for example, the subject specification at page 8).

Although not specifically discussed in the Office Action, the examiner apparently misinterprets "floating point data" to be the same thing as "physics simulation data." Certainly, floating point data and floating point calculations may be an important part of the computational processes used to generate physics simulation data, but these are clearly not equivalent terms. Physics simulation data is data related to one or more physics-related algorithms running on the PPU that implement a physics simulation. In contrast, floating point data is a well known type of data commonly used in many types of computational processes, such as the graphics processing performed by Watanabe. Reaching a conclusion that a conventional co-processor commonly outputting floating point data is the same thing as a specialized hardware device outputting physics simulation data is like concluding that a pile of sheet metal is the same thing as a car.

However, to further highlight the distinction between generic floating point data potentially returned to a CPU by a conventional math co-processor from physics simulation data returned to a host by a PPU, independent claim 1 has been amended to recite in combination, "initiating operation of the PPU to calculate physics simulation data." Similarly, independent claim 10 has been amended to recite in combination, "calculating physics simulation data in the PPU", independent claim 15 has been amended to recite in combination, "making a request for physics simulation data . . . [and] initiating operation of the PPU to calculate the physics simulation data", and independent claim 23 has been amended to recite in combination, "providing a dedicated, hardware-based Physics Processing Unit (PPU) adapted to generate the physics simulation data." Thus, pending claims 1-39 expressly recite some provision of "physics simulation data" in relation to the recited PPU element or its functional operation in a related method.

In this regard, newly added claims 32 through 39 further claim more specific types of physics simulation data and further distinguish the art of record.

Watanabe does not disclose or suggest any device analogous to the claimed PPU. The totality of the description within Watanabe related to "co-processor 108" states that it is "provided <u>only</u> to undertake, chiefly, calculation of floating-point decimals. As a result, various decisions are executed by co-processor 108 and the results of these decisions are transferred to CPU 101: the calculation load on the CPU is thereby lightened." (See, Watanabe at Col 3, line 65 through Col. 4, line 2, emphasis added). To somehow extrapolate and/or impute the entire design and functionality of a PPU from this minimalist statement of generic co-processor use is absurd. Watanabe does not suggest or disclose the presence or use of a PPU and/or the generation of physics simulation data by any element. As such, the stated rejection of claims 1-3, 10, 11, 13-15, 23, 25, 26, 28 and 29 should be withdrawn.

The examiner next concludes that any and all references to a driver in the pending claims are anticipated as being "inherently" disclosed by "the system of Watanabe since it is necessary to have a driver for computer components to work with each other." (See Office Action, end of page 2 over to page 3). This conclusion betrays a complete lack of understanding regarding drivers and/or the actual content of the Watanabe document.

A driver is a program that allows a system CPU to communicate with an attached hardware device, such as a printer, a GPU, a disk drive, or in the context of amended claim 1, for example, - a PPU. Because each of these devices potentially utilizes a unique set of commands, a driver is needed to translate commands from a main application running on the CPU into something that the connected device can understand. In contrast, processor and co-processor combinations (e.g., Intel 80X86/80X87 or Motorola 68881/68882) do not require a "driver" to facilitate interoperability. Indeed, many math co-processors are slaved to their associated processor, and can not fetch instructions from memory, execute program flow instructions, perform input/output operations, manage memory, and so on.

Nothing in Watanabe suggests that co-processor 108 is anything other than a conventional floating-point co-processor. As such, a conclusion that a driver must

inherently be used to facilitate interoperability between CPU 101 and co-processor 108 is nothing short of pure fiction. Quite to the contrary, why would any rationale system designer select a CPU and an associated co-processor for <u>implementation on the same printed circuit board</u> in a stand-alone specialty video game console that requires a driver to facilitate interoperability? (See, Watanabe at Col. 3, lines 9-10). Clearly, they would not. The examiner's inherency conclusion is utterly unsupported by the art of record and motivated solely by consideration of the claimed invention. Watanabe does not disclose, suggest or inherently demand the use of a driver. As such, the stated rejection of claims 1-3, 10, 11, 13-15, 23, 25, 26, 28 and 29 should be withdrawn.

In sum, the Watanabe system is exactly the type of conventional system clearly distinguished in the subject specification, except for the fact that there is no evidence whatsoever that Watanabe actual executes a physics simulation. However, assuming for the moment, as the examiner clearly did, that Watanabe performs some sort of physics related computation, said computation is serially executed by <u>only</u> the CPU 101. That is, in every single instance throughout the entire lengthy discussion presented in Watanabe regarding execution of program steps required to animate the various graphical effects, CPU 101 performs the execution. Every computation step associated with the flowcharts in Watanabe is done in sequence by CPU 101. No other computational device executes a single program step (graphics related or otherwise) in Watanabe. This is certainly true of co-processor 108 which is never identified as independently executing any aspect of the graphics program being run in the Watanabe document. Thus, CPU 101 serially executes all of the graphics, audio, data transfer, and whatever other program steps are required to execute the Watanabe program with the assistance of limited floating-point calculations being run on co-processor 108.

Watanabe does not generate physics simulation data. Watanabe does not include a PPU or any device that can reasonably be said to suggest a PPU. In contrast, Watanabe addresses an issue related to graphics calculations. (Note that graphics data ROM 109 is the only "data" feeding co-processor 108 – see, Watanabe at Col. 3, lines 62-65) The Watanabe system generates animations shortcuts, not the real-time, physics simulation data. Watanabe is utterly unrelated to the subject application and

the stated rejection of claims 1-3, 10, 11, 13-15, 23, 25, 26, 28 and 29 should be withdrawn.

Claims 1-39 distinguish over the art of record and are in condition for allowance.

Respectfully submitted,

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